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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,212	07/24/2003	Christophe F. Pomarede	ASMEX.284C1	9674
20995	7590	04/08/2005	EXAMINER	
KNOBBE MARTENS OLSON & BEAR LLP			LEE, HSIEN MING	
2040 MAIN STREET			ART UNIT	PAPER NUMBER
FOURTEENTH FLOOR				
IRVINE, CA 92614			2823	

DATE MAILED: 04/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/626,212	POMAREDE ET AL. <i>(RM)</i>
	Examiner	Art Unit
	Hsien-ming Lee	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 11 February 2005.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 2,4-6,8-10,12,14,15 and 17-19 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 2,4-6,8-10,12,14,15 and 17-19 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

*HSIEN-MING LEE  
PRIMARY EXAMINER*

*4/6/2005*

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>021105</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Remarks*

1. Applicants' cancellation to claims 1, 3, 7, 11, 13 and 16 is acknowledged. Claims 2, 4-6, 8-10, 12, 14, 15 and 17-19 are pending in the application.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 2, 4, 5, 8-10, 12, 14, 15 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Sneh et al. (US 6,503,330).

In re claim 9, Sneh et al., in Figs. 4-11 and related text, teach the claimed method of depositing a film Al<sub>2</sub>O<sub>3</sub> on a semiconductor surface (i.e. silicon substrate 20) in a partially fabricated integrated circuit, comprising:

- exposing the semiconductor surface 21 to products of a O<sub>2</sub>/H<sub>2</sub>/H<sub>2</sub>O/NH<sub>3</sub> plasma (col. 6, lines 50-54), thereby modifying termination of the semiconductor surface 21, by creating termination sites AH (Fig. 8 and col. 5, line 17), without significantly affecting bulk properties beneath the surface, i.e. the termination sites AH would only activate the surface 21 of the silicon substrate 20 (Figs. 5-8) but do not affect bulk

properties of the semiconductor surface, such as diffusing activated species from the plasma into the silicon substrate 20; and

- after modifying the surface termination, depositing a layer 22 (i.e. Al<sub>2</sub>O<sub>3</sub>, col. 6, lines 47-53) thereover using an atomic layer deposition process (col. 5, lines 39-43), wherein the atomic layer deposition process comprises a metal oxide (i.e. Al<sub>2</sub>O<sub>3</sub>, col. 6, line 53) deposition.

In re claims 2 and 12, Sneh et al. teach that the O<sub>2</sub>/H<sub>2</sub>/H<sub>2</sub>O/NH<sub>3</sub> plasma (col. 6, lines 50-54) comprises a nitrogen-excited species (i.e. NH<sub>3</sub>).

In re claims 4, 5, 14 and 15, Sneh et al. teach that the atomic layer deposition (i.e. ALD) comprises depositing an oxide, such as Al<sub>2</sub>O<sub>3</sub> (col. 6, lines 47-53), having a higher dielectric constant than silicon nitride.

In re claims 8 and 17, Sneh et al. teach that the plasma is generated remote from the surface since the exposing step uses remote plasma process (col. 6, lines 50-51).

In re claim 10, Sneh et al., in Figs. 4-11 and related text, teach the claimed method of depositing a film 22 on a semiconductor surface 21 in a partially fabricated integrated circuit, comprising:

- exposing a top surface 21 to products of a O<sub>2</sub>/H<sub>2</sub>/H<sub>2</sub>O/NH<sub>3</sub> plasma (col. 6, lines 50-54), thereby modifying termination of the semiconductor surface 21 without significantly affecting bulk properties beneath the surface 21; and
- after modifying the surface termination, depositing a layer 22 thereover using an atomic layer deposition process (col. 5, lines 39-43), wherein the atomic layer deposition process comprises two reactant pluses with intervening purge pulses in

each cycle, i.e. comprises two precursors having chemistry A and B, respectively, alternatively being introduced with a carrier gas purge in between each cycle of the introducing (col. 10, lines 44-56).

4. Claims 2, 4, 5, 8-10, 12, 14, 15 and 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Sneh et al. (US 6,551,399).

In re claim 9, Sneh et al., in Figs. 7-8 and related text, teach the claimed method of depositing a film 14 on a semiconductor surface 11 in a partially fabricated integrated circuit, comprising:

- exposing the surface of the semiconductor 11 to products of a NH<sub>3</sub>/H<sub>2</sub>/N<sub>2</sub> plasma (col. 6, lines 43-45), thereby modifying termination of the semiconductor surface, by creating termination sites 18 (Fig. 7), without significantly affecting bulk properties beneath the surface, i.e. the termination sites 18 would only activate the surface of the semiconductor 11 but do not affect bulk properties of the semiconductor surface; and
- after modifying the surface termination, depositing a layer 14 thereover (Fig. 8) using an atomic layer deposition process (col. 5, lines 12-13), wherein the atomic layer deposition process comprises a metal oxide (i.e. Al<sub>2</sub>O<sub>3</sub>, col. 5, lines 12-13) deposition.

In re claims 2 and 12, Sneh et al. teach that the NH<sub>3</sub>/H<sub>2</sub>/N<sub>2</sub> plasma (col. 6, lines 43-45) comprises a nitrogen-excited species.

In re claims 4, 5, 14 and 15, Sneh et al. teach that the atomic layer deposition (i.e. ALD) comprises depositing an oxide, such as Al<sub>2</sub>O<sub>3</sub> (col. 5, lines 12-15), having a higher dielectric constant than silicon nitride.

In re claims 8 and 17, Sneh et al. teach that the plasma is generated remote from the surface since the exposing step uses remote plasma process (col. 9, lines 9-10).

In re claim 10, Sneh et al., in Figs. 7-8 and related text, teach the claimed method of depositing a film 14 on a semiconductor surface 11 in a partially fabricated integrated circuit, comprising:

- exposing a top surface 11 to products of a NH<sub>3</sub>/H<sub>2</sub>/N<sub>2</sub> plasma (col. 6, lines 43-45), thereby modifying termination of the semiconductor surface 11 without significantly affecting bulk properties beneath the surface 11; and
- after modifying the surface termination, depositing a layer 14 thereover using an atomic layer deposition process (col. 5, lines 12-13), wherein the atomic layer deposition process comprises two reactant pluses with intervening purge pulses in each cycle, i.e. comprises two precursors alternatively being introduced with a carrier gas purge in between each cycle of the introducing (col. 13, lines 1-9).

In re claims 18 and 19, Sneh et al., in Figs. 7-8 and related text, teach the claimed method of depositing a film 14 on a semiconductor surface 11 in a partially fabricated integrated circuit, comprising:

- exposing the surface 11 to a NH<sub>3</sub>/H<sub>2</sub>/N<sub>2</sub> plasma (col. 6, lines 43-45), thereby modifying termination of the semiconductor surface 11 without depositing greater than one atomic monolayer of the products of the plasma on the surface (col. 3, lines 49-53); and
- after modifying the surface termination, depositing a layer 14 thereover using an atomic layer deposition process (col. 5, lines 12-13), wherein the atomic layer

deposition process comprises a metal oxide (i.e. Al<sub>2</sub>O<sub>3</sub>, col. 5, lines 11-14) deposition, wherein the atomic layer deposition process comprises two reactant pulses with intervening purge pulses in each cycle (col. 13, lines 1-9).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sneh et al. (US '399) in view of Sneh et al. (US 6,503,330).

In re claim 6, Sneh et al. teach the claimed method of depositing a film 14 on a semiconductor surface 11 in a partially fabricated integrated circuit, comprising:

- exposing the surface 11 to products of a NH<sub>3</sub>/H<sub>2</sub>/N<sub>2</sub> plasma, thereby modifying termination of the semiconductor surface 11 without significantly affecting bulk properties beneath the surface; and
- after modifying the surface termination, depositing a layer 14 thereover using an atomic layer deposition process.

Sneh (US '399) et al. do not expressly teach that the exposing step incorporates less than 10 atomic % of the products of the plasma at a depth of less than about 10 Å from the surface.

Sneh et al. (US '330), however, in an analogous art, suggested that using plasma for modifying the surface termination would involve a formation of self-saturated layer, which is approximately 5 angstroms thick (col. 6, lines 62-67).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to recognize that by routine optimization to incorporates a desired atomic percentage of the products of the plasma in the method of Sneh (US '399), to form a thin layer at a depth less than 10 angstroms from the surface , as taught by Sneh '330. The motivation/suggestion for doing so is to form a very thin self-saturated layer on the semiconductor surface, which would be beneficial to produce an uniform layer formed on the semiconductor surface that has been treated by the plasma (col. 5, lines 26-38, Sneh '330).

***Claim Rejections - 35 USC § 112***

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 6 recites the limitation " greater than about 10 Å from the surface " in line 9.

There is insufficient antecedent basis in the written specification for supporting the limitation claim.

On paragraphs [0084] and [0101] of the originally specification, it discloses that the depth (i.e. the thickness of interface 262) is of 10 Å or less than 10 Å. For the foregoing reason, the rejection against claim 6 is based on the disclosure on paragraphs [0084] and [0101] of the specification, i.e. the depth is about less than 10 Å.

***Response to Arguments***

9. Applicant's arguments filed 2/11/2005 have been fully considered but they are not persuasive.

Applicant's arguments is on the ground that Sneh '399 does not teach modifying termination of the *semiconductor* surface because Sneh'399 discloses modifying termination of the dielectric surface 14 as shown in Fig.9.

In response to the argument, while it is true that the dielectric surface 14 is modified as shown in Fig.9, Sneh'399 also teach modifying termination of the *semiconductor* surface 11 (Fig.7) to create termination sites 18 thereon prior to depositing the dielectric layer 14. The teachings of Sneh'399 as a whole still read on the claims.

Sneh'330 is used to remedy the deficiency in Sneh '399, as stated previously. By this combination, it would be beneficial to produce an uniform layer on the plasma-treated surface, as stated previously.

In fact, Sneh'330 expressly teach modifying termination of the *semiconductor* surface 21 (i.e. the surface 21 of a silicon substrate 20) followed by depositing a Al<sub>2</sub>O<sub>3</sub> layer thereon, as stated previously.

Since Sneh'330 teaches all and each claimed limitations as recited in claims 2, 4, 5, 8-10, 12, 14, 15 and 17; Sneh '399 teaches all and each claimed limitations as recited in claims 2, 4, 5, 8-10, 12, 14, 15 and 17-19 and Sneh '399 in view of Sneh '330 read on claim 6, the rejections are deemed proper.

*Conclusion*

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (8:00 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee  
Primary Examiner  
Art Unit 2823

HSIEN-MING LEE  
PRIMARY EXAMINER

April 6, 2005

4/6/2005